Waveform Sampling, PSEC4 ASIC, & DAQ

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Why waveform sampling?

Advantages:

• Preserve full signal information: timing and charge
• Understand noise, ability to subtract noise and manipulate signal in frequency space, etc
• Pile-up / ‘defective’ pulse detection
• Low power*

Challenges:

• Large amount of data throughput required
• Calibrations, calibrations, calibrations...(calibrations)**

*Low power if not using Flash ADC or other continuous digitizer for front-end option .
** more calibrations
Waveform Sampling ASICs

- Already in use in many experiments...

LABRADOR3, ANITA Experiment

SAM, H.E.S.S.-II

DRS4, MEG Experiment
### Waveform Samplers 'on the market':

<table>
<thead>
<tr>
<th>ASIC</th>
<th>Amplification?</th>
<th># chan</th>
<th>Depth/chan</th>
<th>Sampling [GSa/s]</th>
<th>Vendor</th>
<th>Size [nm]</th>
<th>Ext ADC?</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRS4</td>
<td>no.</td>
<td>8</td>
<td>1024</td>
<td>1-5</td>
<td>IBM</td>
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<tr>
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<tr>
<td>IRS2</td>
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<td>32536</td>
<td>1-4</td>
<td>TSMC</td>
<td>250</td>
<td>no.</td>
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<td>BLAB3A</td>
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<td>1-4</td>
<td>TSMC</td>
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<tr>
<td>TARGET</td>
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<td>TSMC</td>
<td>250</td>
<td>no.</td>
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<tr>
<td>TARGET2</td>
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<td>16384</td>
<td>1-2.5</td>
<td>TSMC</td>
<td>250</td>
<td>no.</td>
</tr>
<tr>
<td>TARGET3</td>
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<td>16</td>
<td>16384</td>
<td>1-2.5</td>
<td>TSMC</td>
<td>250</td>
<td>no.</td>
</tr>
<tr>
<td>PSEC3</td>
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<td>256</td>
<td>1-16</td>
<td>IBM</td>
<td>130</td>
<td>no.</td>
</tr>
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<td>PSEC4</td>
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<td>6</td>
<td>256</td>
<td>1-16</td>
<td>IBM</td>
<td>130</td>
<td>no.</td>
</tr>
</tbody>
</table>
Design: PSEC4

- 10-15 Gsa/s Switched capacitor array array sampling
- ‘analog down-conversion’:
  
  GHz sampling $\rightarrow$ 10-100 MHz readout rate
- useful in most triggered event applications
- Configurable: user can set ADC resolution, digitization time, sampling rate, region of interest readout block.
- Up-convert low frequency (~10’s MHz) clock to multi-GHz using tapped delay line:

\[ \text{locked sampling } @ 10\text{GSa/s w/ on chip DLL} \]
Design: PSEC4

- PSEC4 design was targeted to the characteristics of fast MCP pulses
- High bandwidth and high sampling rate
- Trade-off: small recording window [25 ns when sampling at 10.24 GSa/s]
- PSEC5 design has begun: merge PSEC4 performance capabilities with a deeper buffer sampling chip
1) Design: How PSEC4 (and similar chips) operate

- *PSEC-3 timing shown (roughly the same), though PSEC-4 can run readout 2x faster – highly serial...
1) Design: How PSEC4 works

Sampling

Write_clock [40MHz]

Self_trigger

Trigger_threshold

Ext. Trigger

ADC start/stop

Data[12..1]

Data_address

Read_clock

Signal

50Ω

V_ped
1) Design: How PSEC4 works

Digitization (parallel)
1) Design: How PSEC4 works

Readout (serial)
2) Performance: calibrations

*Oscilloscope on a chip?* Not quite...a modified approximation:

For example, a raw PSEC-3 readout (10 GS/s) of 120 MHz, 150 mV\(_{rms}\) sine wave:
2) Performance: calibrations

- Voltage pedestals
- ADC non-linearity
- Time-base non-linearity

3/2/2014 ANNIE workshop
2) Performance: calibrations

Want to minimize number of calibration steps!
Other calibrations/stability considerations: temperature effects on digitizer baseline

![Graph showing temperature effects on digitizer baseline]

- Pedestal: CH.3 cell 120
- Linear fit: -8.3 ADC counts/°C

3/2/2014 ANNIE workshop
Other calibrations/stability considerations: temperature on DC transfer curves
Good intra-chip timing after calibrations (waveform fitting)
PSEC4 compared to deeper buffer samplers

PSEC4:
- DLL
- Timing Control Logic
- Primary Sampling Array (256)
- On-chip trigger
- Digitization Block (256)
- 12-bit Parallel Readout
- Data Out

Deeper Buffer Samplers:
- DLL
- Timing Control Logic
- Primary Sampling Array (2x128)
- On-chip trigger
- Fan-out buffers (256)
- Long-term analog storage: 128 x 256 cells
- Write & Read Address
- Digitization Block (256)
- Data Serializer
- High-speed LVDS readout
- Data Out
PSEC4 compared to deeper buffer samplers

<table>
<thead>
<tr>
<th>Parameter</th>
<th>PSEC4</th>
<th>PSEC5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channels</td>
<td>6</td>
<td>4</td>
</tr>
<tr>
<td>Sampling Rate</td>
<td>4-15 GSa/s</td>
<td>5-15 GSa/s</td>
</tr>
<tr>
<td>Primary Samples/channel</td>
<td>256</td>
<td>256</td>
</tr>
<tr>
<td>Total Samples/channel</td>
<td>256</td>
<td>32768 [3.3 μs]</td>
</tr>
<tr>
<td>Recording Buffer Time at 10 GSa/s</td>
<td>25.6 ns</td>
<td>3.3 μs</td>
</tr>
<tr>
<td>Analog Bandwidth</td>
<td>1.5 GHz</td>
<td>1.5 - 2 GHz</td>
</tr>
<tr>
<td>RMS Voltage Noise</td>
<td>700 μV</td>
<td>&lt;1 mV</td>
</tr>
<tr>
<td>DC RMS Dynamic Range</td>
<td>10.5 bits</td>
<td>10 - 11 bits</td>
</tr>
<tr>
<td>Signal Voltage Range</td>
<td>1 V</td>
<td>1 V</td>
</tr>
<tr>
<td>ADC on-chip</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>ADC Clock Speed</td>
<td>1.4 GHz</td>
<td>1.5 - 2 GHz</td>
</tr>
<tr>
<td>Readout Protocol</td>
<td>12-bit parallel</td>
<td>serial LVDS: one per channel</td>
</tr>
<tr>
<td>Readout Clock Rate</td>
<td>40 MHz</td>
<td>500 MHz</td>
</tr>
<tr>
<td>Average Power Consumption</td>
<td>100 mW</td>
<td>300-500 mW</td>
</tr>
<tr>
<td>Core Voltage</td>
<td>1.2 V</td>
<td>1.2 V</td>
</tr>
</tbody>
</table>

Also, for comparison: Gary Varner’s IRS (Ice-Radio Sampler) series of ASICs samples 4 GSa/s with $2^{15}$ storage cells ~ 8 microseconds of continuous waveform recording
Deeper buffer (PSEC5 and related Hawai‘i ASICs)

- Potential for ‘dead time-less’ operation depending on chip sampling rate, readout rate, and experiment trigger rate
Deeper buffer (PSEC5 and related Hawai‘i ASICs)

- Storage in analog memory in a block of N cells, where this corresponds to a time window of N * [sampling rate]^{-1}
- Ability to digitize and readout this window of interest, and still actively sample the detector. (i.e. ability to record both prompt Cherenkov and delayed scintillation)
DAQ

• Our Chicago group has designed an LAPPD glass-package DAQ system based on the PSEC4 chip.
Firmware flow for ASIC control

PSEC4 timing

Trigger handling

ADC feedback

RAM

DAQ upstream
Front-end PSEC4 card <-> Central Card communication

- Eight 800 Mbps LVDS pairs
- Data, clock, trigger, configuration
- Front-end card houses 5 PSEC4 chips (30 channels)
- Newest board revision has optional mezzanine plug-in for adding a gain stage
Simple event waveform viewer

Trigger board using CH. 6 of ASIC[0]

Open waveform viewer: (refreshes on enter)
LAPPD Demountable System Testing @ APS
Dual-end PSEC4 pulse recording (10 strips):
Dual-end PSEC4 pulse recording (10 strips):

Pulse Height dist. (ADC counts)

Charge centroiding for transverse resolution
Experiment/simulation driven DAQ design

- What are properties of expected signals from PMTs and LAPPDs? (Bandwidth, pulse height, NPE, etc)
- What are the time distributions of photon hits on the detectors?
- What system time resolution is adequate?
- How to form a system trigger? How fast?
The End